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IN THE CLAIMS

**Claims 1-20 (canceled)**

**Claim 21 (previously presented): An FET device comprising:**

    a substrate with a top substrate surface upon which a gate electrode stack is formed;  
    said gate electrode stack comprising a gate electrode formed over a gate dielectric layer, said gate dielectric layer being formed on said top substrate surface;  
    said gate electrode being composed of gate polysilicon and having a top gate electrode surface and having gate electrode sidewalls with a cap formed over said top gate electrode surface;  
    sidewall spacer material formed on said gate electrode sidewalls aside from said gate electrode;  
    said cap layer having outer edges and a top formed in said top gate electrode surface, said cap layer comprising an amorphous silicon layer formed in said top surface of said gate polysilicon;  
    notches formed in said outer edges of said cap layer recessed from said gate electrode sidewalls;  
    said notches in said outer edges of said cap layer having been filled with protective plugs formed on said top of said gate electrode layer;  
    said sidewall spacer material reaching along said gate electrode sidewalls to above a level at which said protective plugs contact said polysilicon of said gate electrode whereby said sidewall spacer material is contiguous with and overlapping said protective plugs covering said sidewalls of said gate electrode; and  
    an epitaxial, raised source region and an epitaxial, raised drain region formed on top of said top substrate surface of said substrate aside from said sidewall spacer material.

**Claim 22 (canceled)**

**Claim 23 (previously presented): The FET device of claim 21 wherein said protective plugs and said sidewall spacer material comprise a dielectric material.**

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**Claim 24 (previously presented): The FET device of claim 22 wherein said protective plugs and said sidewall spacer material comprise a dielectric material.**

**Claim 25 (previously presented): The FET device of claim 21 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.**

**Claim 26 (previously presented): The FET device of claim 22 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.**

**Claim 27 (previously presented): The FET device of claim 23 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.**

**Claim 28 (previously presented): The FET device of claim 24 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.**

**Claim 29 (previously presented): The FET device of claim 21 wherein said cap layer comprises an implanted region formed in said polysilicon of said gate electrode, said amorphous silicon region having been implanted with a material selected from the group consisting of silicon and germanium.**

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**Claim 30 (previously presented): An FET device comprising:**

**a semiconductor substrate with a top substrate surface upon which a gate electrode stack is formed;**

**said gate electrode stack comprising a gate electrode formed over a gate dielectric layer, said gate dielectric layer being formed on said top substrate surface;**

**said gate electrode being composed of polysilicon and having a top surface and having gate electrode polysilicon sidewalls;**

**sidewall spacer material formed on said gate electrode polysilicon sidewalls aside from said gate electrode;**

**a raised source region and a raised drain region source/drain regions formed on top of said substrate surface aside from said sidewall spacer material;**

**an implanted cap layer having outer edges and a top formed in said top surface of said gate electrode comprising an ion implanted layer formed in said polysilicon of said gate electrode, said polysilicon in said cap layer having been implanted with a material selected from the group consisting of silicon and germanium;**

**notches formed in said outer edges of said implanted cap layer recessed from said gate electrode sidewalls;**

**said notches in said outer edges of said implanted cap layer having been filled with said sidewall spacer material forming protective plugs on said top of said gate electrode;**

**said sidewall spacer material being contiguous with and overlapping said protective plugs covering said gate electrode polysilicon sidewalls of said gate electrode;**

**said sidewall spacer material reaching along said gate electrode sidewalls to above a level at which said protective plugs contact said gate electrode polysilicon; and**

**an epitaxial, raised source region and an epitaxial, raised drain region formed on top of said top substrate surface of said substrate aside from said sidewall spacer material.**

**Claim 31 (canceled)**

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**Claim 32 (previously presented):** The FET device of claim 30 wherein [::] said substrate comprises a Silicon On Insulator (SOI) structure.

**Claim 33 (canceled)**

**Claim 34 (previously presented):** The FET device of claim 32 wherein said protective plugs are formed of said sidewall spacer material which comprises a dielectric.

**Claim 35 (previously presented):** The FET device of claim 30 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.

**Claim 36 (canceled)**

**Claim 37 (previously presented):** The FET device of claim 32 wherein said cap and said protective plugs have top surfaces covered by a hard mask layer.

**Claim 38 (canceled)**

**Claim 39 (previously presented):** The FET device of claim 34 whercin:  
said substrate comprises a Silicon On Insulator (SOI) structure; and  
said cap layer comprises an ion implanted layer formed in said polysilicon of said gate electrode.

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**Claim 40 (previously presented): A SOI MOSFET device comprising:**

**a silicon semiconductor layer has a top surface with a gate electrode stack formed on said top surface of said silicon layer;**

**said gate electrode stack comprises a gate dielectric layer formed on said surface of said silicon layer and a gate electrode with a top formed on said gate dielectric layer;**

**said gate electrode being composed of gate polysilicon having a top surface and having polysilicon sidewalls with a cap formed on top of said gate polysilicon, said cap having a periphery;**

**sidewall spacer material formed on said polysilicon sidewalls of said gate electrode;**

**said cap being formed of amorphous silicon implanted with a material selected from the group consisting of silicon and germanium;**

**a hard mask formed on top of said cap;**

**said cap being undercut in said periphery of said cap in the form of a notch above said gate electrode and below said hard mask;**

**said notch having been filled with said sidewall spacer material forming dielectric plugs between said gate electrode and said cap to prevent exposure of said gate polysilicon of said gate electrode;**

**said sidewall spacer material reaching along said sidewalls of said gate electrode and overlapping said plugs; and**

**an epitaxial, raised source region and an epitaxial, raised drain region formed on top of said top surface of said silicon layer aside from said sidewall spacer material.**